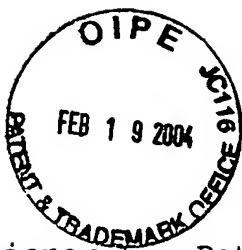


TSMC-03-373



February 9, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: | Serial No. 10/719,722 11/21/03 |

Wen-Ting Chu et al.

A METHOD TO FORM FLASH MEMORY WITH
VERY NARROW POLYSILICON SPACING

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.


The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450, on February 17, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

 2/17/04



SMC-03-373

U.S. Patent 6,342,451 to Ahn, "Method of Fabricating Floating Gates in Semiconductor Device," discloses methods to form a floating gate. Sidewall spacers are used to define a floating gate pattern.

U.S. Patent 6,514,868 to Hui et al., "Method of Creating a Smaller Contact Using Hard Mask," teaches a method to form a contact hole. A tapered hard mask is used to define a contact hole opening.

U.S. Patent 6,177,331 to Koga, "Method for Manufacturing Semiconductor Device," teaches an integrated circuit manufacturing method where a hard mask is tapered.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Group Art Unit

U. S. PATENT DOCUMENTS

PLUNK DATE
IF APPROPRIATE

Translation

YES	NO
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DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.